

Substitute for Form 1449A/PTO (M ¹) (use as many sheets as necessary)		Attorney Docket No.: 042390P3495C2	Application Number: 09/274,430
Page 1 of 11		First Named Inventor: Michael Barrow	
		Filing Date: March 22, 1999	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
		4,887,148		Mu	12/12/1989	
		5,216,278		Lin et al.	6/1/1993	
		5,285,352		Pastore et al.	2/8/1994	
		5,355,283		Marrs et al.	10/11/1994	
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		5,450,283		Lin et al.	9/12/1995	
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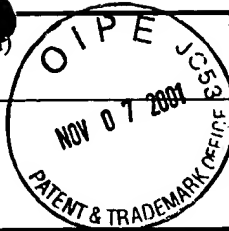
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Application Number:
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First Named Inventor:
Michael Barrow
Filing Date:
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OTHER ART - NO PATENT LITERATURE DOCUMENTS

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<i>JB</i>		1991 Proceedings, 41 st Electronic Components & Technology Conference, May 11-16, 1991, Atlanta, Georgia	
		Bruce Freyman et al., "Surface Mount Process Technology for Ball Grid Array Packaging, Amkor Electronics Inc., Tempe, Arizona, pgs. 81-85	
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		Dave Hattas, "BGAs Face Production Testing", Advanced Packaging, Summer 1993, pgs. 44-46	
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		Randy Johnson et al., "Ball Grid Array Technology: A Feasibility Study of Ball Grid Array Packaging", Nepcon Conference, Proceeding of the Technical Program, June 14-17, 1993 Boston Massachusetts, pgs 411-430	
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		Leo Anderson et al., " Solder Attachment Analysis of Plastic BGA Modules", Surface Mount International, San Jose, CA, August 1994, pgs. 189-194	
		Dr. Abbas I. Attarwala et al., "Failure Mode Analysis of a 540 Pin Plastic Ball Grid Array", Surface Mount International, San Jose, CA, August 1994, pgs. 252-257	

Examiner Signature	<i>John B. Vigneri</i>	Date Considered	<i>09/09/02</i>
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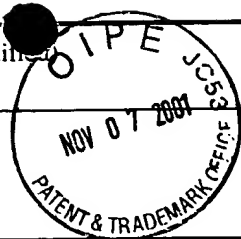
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Page 3 of 11	First Named Inventor: Michael Barrow	Filing Date: March 22, 1999



OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
26		Surface Mount International Conference & Exposition: Proceedings of The Technical Program, San Jose, CA, Aug 28-Sept 1, 1994	
27		C.E. Bauer, "Partitioning and Die Selection Strategies for Cost Effective MCM Designs"; W.E. BERNIER et al., "BGA vs QFP: A Summary of Tradeoffs for Selection of High I/O Components"; A.J. MAWER et al., "Plastic Ball Grid Array Solder Joint Reliability Considerations"; Dr. W.C. Mak et al., "Increased SOIC Power Distribution Capability Through Board Design and Finite Element Modeling", Journal of Surface Mount Technology, October 1994	
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36		Charles L.Hutchins "Understanding Grid Array Packages", Surface Mount Technology Magazine, November 1994, pgs 12-13	
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Examiner Signature	<i>John F. Vogt</i>	Date Considered	09/09/02
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39		John H. Lau et al. "No Clean Mass Reflow of Large Plastic Ball Grid Array Packages", Journal of Surface Mount Technology, pgs 3-14, July 1994	
40		Charles E. Bauer, Ph.D. et al., "Partitioning and Die Selection for Cost Effective MCM Designs", pgs 4-9; W.E. Bernier et al., "BGA vs QFP: A Summary of Tradeoffs for Selection of High I/O Components", pgs 10-15; Andrew J. Mawer et al. "Plastic Ball Grid Array Solder Joint Reliability Considerations", pgs 16-32; Dr. W.C. Mak et al. "Increased SOIC Power Dissipation Capability Through Board Design and Finite Element Modeling", pgs 33-42, Journal of Surface Mount Technology, October 1994	
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45		Joel Mearig, "An Overview of Manufacturing BGA Technology", Proceeding of the Technical Program, Nepcon West '95 Conference, Feburary/March 1995, Anaheim, CA, pgs 295-299	
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47		Shailesh Mulgaonker et al., "An Assessment of the Thermal Performance of the PBGA Family", IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A. Vol. 18. No 4., December 1995, pgs 739-748	
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49		Reader Service: Hewlett Packard, Actel, Mini-Circuits; Electronic Design, April 1995, Vol. 43, No. 8; Nikkei Microdevices Magazine, Various Articles	

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SPV		Nikkei Microdevices, March 1995, Various Articles	
SI		John H. Lau, "Ball Grid Array Technology" Publication, pgs 1-636	
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S6		Wayne Huang et al. "Electrical Characterization of PBGA for Communication Applications by Simulation and Measurement" Proceeding of the Technical Program, Nepcon West '95, Conference February/March 1995, Anaheim, CA, pgs 307	
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S8		Microprocessor Report, November 1995, Vol. 9, No. 15, Michael Slater "Intel Boosts Pentium Pro to 200 MHz", "AMD Buys NexGen to Boost x86 Position"; Linly Gwennap "Integrated PA-7300LC Powers HP Midrange", "UltraSparc to Pick Up Speed in 1996"; Jim Turley "StrongArm Punches Up ARM Performance"; Brian Case "First Trimedia Chip Boards PCI Bus"; and Mike Johnson "RISC-like Design Fares Well for x86 CPUs	
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61		T. Kawahara et al. "Ball Grid Array Type Package by Using of New Encapsulation Method", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 1995	

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JW		John U. Knickerbocker et al., "Materials: Ceramic BGA" Advanced Packing Magazine, January/February 1995, pgs 20-25	
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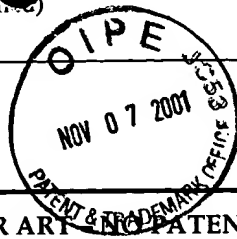
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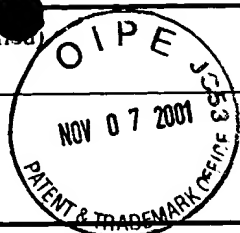
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		Bruce Freyman et al., "The Move to Perimeter Plastic BGA's" Surface Mount International, Proceedings of the Technical Program, San Jose, CA, August 1995	
		Bruce M. Guenin et al., "Analysis of a Thermally Enhanced Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part A, Vol. 18, No. 4, December 1995, pp 749-757	
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		Semiconductor Group Package Outlines Reference Guide, Texas Instruments Incorporated, 1995	
		Shailesh Mulgaonker et al., "An Assessment of the Thermal Performance of the PBGA Family", 1995 Proceedings, Eleventh IEEE Semiconductor Thermal Measurement and Management Symposium, pp 17-27	
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BV		Ed Zamborsky, "BGAs in the Assembly Process", Circuits Assembly, Vol. 6, No. 2, February 1995, pp 60-64	
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Examiner Signature	<i>John B. Vignati</i>	Date Considered	09/09/02
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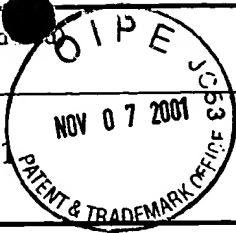
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Page No. 17

Substitute for Form 1449A/PTO (Model 1449A) (use as many sheets as necessary)	Attorney Docket Number 042390P3495C2	Application Number: 09/274,430
Page 10 of 11	First Named Inventor: Michael Barrow	Filing Date: March 22, 1999



OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, city and/or country where published	Translation ²
<i>AB</i>		Michael Barrow, "Perimeter Matrix Ball Grid Array Circuit Package with a Populated Center", International Search Report, PCT/US97/03511, March 1996	
		LSI Logic Corporation, Package Selector Guide, 1991-1995	
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		Randy Johnson et al., "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", Nepcon East '93 Conference, Boston, Ma, June 1993	
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		Andrew J. Mawer et al., "Plastic Ball Grid Array Solder Joint Reliability Considerations", Surface Mount Technology Association, Journal of Surface Mount Technology, October 1994, pp 16-32	
<i>✓</i>		Dr. W.C. Mak et al., "Increased SOIC Power Dissipation Capability Through Board Design and Finite Element Modeling" Surface Mount Technology Association, Journal of Surface Mount Technology, October 1994, pp 33-41	

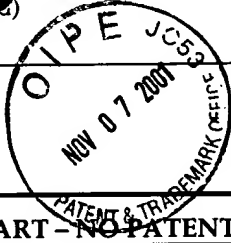
Examiner Signature <i>John B. Vignata</i>	Date Considered 09/09/02
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JBR		Philip E. Rogren, "MCM-L Built on Ball Grid Array Formats", Surface Mount International, Proceedings of the Technical Program, San Jose, Ca, August/September 1994	
		James J. Clementi et al., "Flip-Chip Assembly on CQFP Using No-Clean Processing" Proceedings 1995 International Flip Chip, Ball Grid Array, Tab and Advanced Packaging Symposium, San Jose, Ca, February 1995	
		Andrew Mawerand et al., "Reliable BGAs Take on Extra Routes" Electronic Engineering Times 98, Interconnects & Packaging, Issue 816, September 1994	
		Johnathan L. Houghten, "Plastic Ball-Grid Arrays Continue to Evolve", February 6, 1995 issue of Electronic Design, Vol. 43, No. 3, pgs 5, 7, 141-146, Penton Publishing Inc., Cleveland, OH	
		Compaq, "Compaq's Proposed BGA Package for Low Cost High Volume Products" (one page), November 8, 1993	
		LSI Logic, Package Selector Guid 1994-1995, cover page, chapter cover page, pgs 8-27 and 8-31	
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		BGA Product Guide Updates, Amkor/Anam, June 1994	
		Steve Liew et al., Fax to Mike Barrow regarding BGA Details, December 21, 1994, pgs 1-2	

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MAY 24 2002

Application Number	09/274,430
Filing Date	March 22, 1999
First Named Inventor:	Michel Barrow
Group Art Unit	2841
Examiner Name	David A. Foster
Attorney Docket Number	042390P3495C2

Sheet **1** of 2

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